AMENDMENT TO THE CLAIMS

Please amend the presently pending claims as follows:

1. (Currently Amended) Integrated circuit comprising means of delivering to at least one output a predetermined output voltage representative of a logic level, which ~~the integrated circuit comprising~~ comprises means of ~~distributing~~ generating a ~~mains~~ main voltage and means of generating an internal reference voltage lower than the ~~mains~~ main voltage, characterized in that it comprises

means of ~~connection~~ connecting ~~to the mains~~ the main voltage on the output, and

means of limiting and/or detecting the voltage on the output at the value of the predetermined output voltage, equal to the internal reference voltage, taking into account the reference voltage.

2. (Cancelled)

3. (Currently Amended) Integrated circuit according to claim 2, characterized in that, when the predetermined voltage is reached, the currents circulating in the connecting means ~~of connecting the mains voltage~~ and in the limiting and/or detecting means ~~of limiting and/or detecting the voltage~~ are balanced.

4. (Currently Amended) Integrated circuit according to claim 2, characterized in that the ~~connection~~ connecting means comprise a first power transistor.

5. (Currently Amended) Integrated circuit according to claim 4, characterized in that the drain of the ~~primary~~ first power transistor is connected to the output and its source to the ~~mains~~ main voltage.

6. (Currently Amended) Integrated circuit according to claim 2, characterized in that the limiting means ~~of limiting the voltage~~ comprise at least a second transistor controlled on its gate by the reference voltage.

7. (Original) Integrated circuit according to claim 6, characterized in that the gate of the second transistor is connected to the gate of a third transistor mounted in a diode at the reference voltage.

8. (Currently Amended) Integrated circuit according to claim 4, characterized in that the limiting means ~~of limiting the voltage~~ comprise means of blocking the first power transistor when the predetermined voltage is reached.

9. (Original) Integrated circuit according to claim 8, characterized in that the blocking means have first and second current mirrors connected to each other.

10. (Currently Amended) Integrated circuit according to claim 9, characterized in that the first current mirror delivers a blocking current when the predetermined voltage is reached on the output, and in that the second mirror sends a copy of the blocking

current to the gate of the first power transistor, so as to block it.

11. (Currently Amended) Integrated circuit according to claim 4, characterized in that the gate of the first power transistor is connected to a command input via a fourth transistor.

12. (Currently Amended) Integrated circuit according to claim 10, characterized in that the power of the ~~third~~ fourth transistor is less than that of the transistors of the second mirror, so that the latter imposes its level on the ~~third~~ fourth transistor when it delivers the copy of the blocking current.

13. (Original) Integrated circuit according to claim 1, characterized in that the output voltage corresponds to the logic level "1" of a USB connection.

14. (Original) Integrated circuit according to claim 1, characterized in that the reference voltage is used to supply the logic CMOS section of the integrated circuit.

15. (Currently Amended) Integrated circuit according to claim 1, characterized in that the reference voltage and/or the predetermined voltage have the value of 3 V, the ~~mains~~ main voltage having a value of 5 V.

16. (Currently Amended) Communication module for ~~th~~an integrated circuit comprising means of delivering, on at least

one output, a predetermined output voltage representative of a logic level, ~~the integrated circuit~~ which comprise means of ~~distributing a mains~~ generating a main voltage and means of generating an internal reference voltage lower than the ~~mains~~ main voltage, characterized in that it comprises

means of connecting the ~~mains~~ main voltage to the output, and

means of limiting the voltage ~~at~~on the output at the predetermined output voltage value, taking into account the reference voltage.

17-20.(Cancelled)

21.(New) Integrated circuit comprising means of delivering to at least one output a predetermined output voltage representative of a logic level, which comprise means of generating a main voltage and means of generating an internal reference voltage lower than the main voltage, characterized in that it comprises

means of connecting the main voltage on the output, which comprise a first power transistor, and

means of limiting and/or detecting the voltage on the output at the value of the predetermined output voltage, taking into account the reference voltage,

the limiting means comprising means of blocking the first power transistor when the predetermined voltage is reached,

the blocking means have first and second current mirrors connected to each other,

the first current mirror delivers a blocking current when the predetermined voltage is reached on the output, and in that the second mirror sends a copy of the blocking current to the gate of the first power transistor so as to block it,

the gate of the first power transistor being connected to a command input via a fourth transistor,

the power of the fourth transistor is less than that of the transistors of the second mirror, so that the later imposes its level on the fourth transistor when it delivers the copy of the blocking current.

22. (New) Integrated circuit comprising means of delivering to at least one output a predetermined output voltage representative of a logic level, which comprise means of generating a main voltage and means of generating an internal reference voltage lower than the main voltage, characterized in that it comprises

means of connecting the main voltage on the output,

and

means of limiting and/or detecting the voltage on the output at the value of the predetermined output voltage, taking into account the reference voltage,

and in that the reference voltage is used to supply a logic CMOS section of the integrated circuit.

23.(New) Integrated circuit comprising means of delivering to at least one output a predetermined output voltage representative of a logic level, which comprise means of generating a main voltage and means of generating an internal

reference voltage lower than the main voltage, characterized in that it comprises

means of connecting the main voltage on the output,

and

means of limiting and/or detecting the voltage on the output at the value of the predetermined output voltage, taking into account the reference voltage,

the means of limiting the voltage comprising at least a transistor controlled on its gate by the reference voltage.